MQFL-28-6R5D

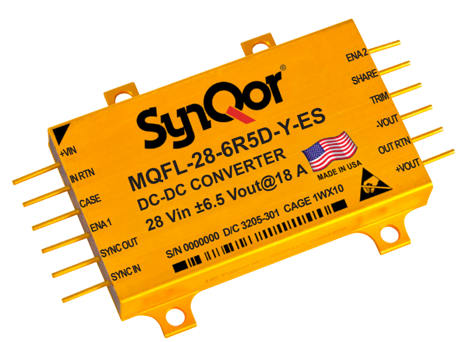
Dual Output

High Reliability DC-DC Converter

16-40 V	16-50 V	±6.5 V	18 A	91% @ 9 A / 90% @ 18 A
Continuous Input	Transient Input	Output	Output	Efficiency

Full Power Operation: -55 ºC to +125 ºC

The MilQor® series of high-reliability DC-DC converters brings SynQor's field proven high-efficiency synchronous rectifier technology to the Military/Aerospace industry. SynQor's innovative QorSeal® packaging approach ensures survivability in the most hostile environments. Compatible with the industry standard format, these converters operate at a fixed frequency, have no opto-isolators, and follow conservative component derating guidelines. They are designed and manufactured to comply with a wide range of military standards.



Designed & Manufactured in the USA
Featuring QorSeal® Hi-Rel Assembly

Design Process

MQFL series converters are:
- Designed for reliability per NAVSO-P3641-A guidelines
- Designed with components derated per:
  - — MIL-HDBK-1547A
  - — NAVSO P-3641A

Qualification Process

MQFL series converters are qualified to:
- MIL-STD-810F
  - — consistent with RTCA/D0-160E
- SynQor's First Article Qualification
  - — consistent with MIL-STD-883F
- SynQor's Long-Term Storage Survivability Qualification
- SynQor's on-going life test

In-Line Manufacturing Process

- AS9100 and ISO 9001 certified facility
- Full component traceability
- Temperature cycling
- Constant acceleration
- 24, 96, 160 hour burn-in
- Three level temperature screening

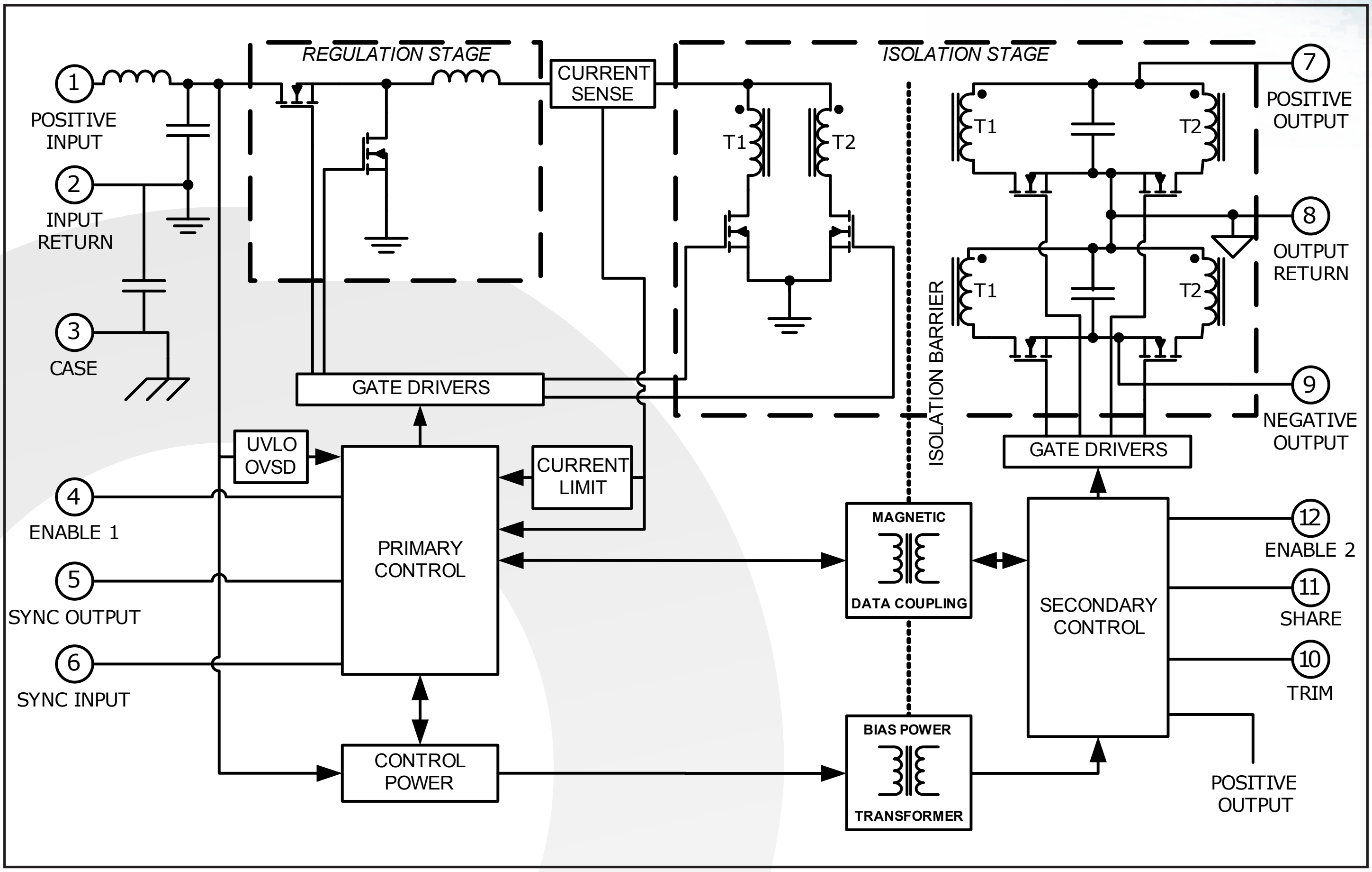
Features

- Fixed switching frequency
- No opto-isolators
- Parallel operation with current share
- Clock synchronization
- Primary and secondary referenced enable
- Continuous short circuit and overload protection
- Input under-voltage and over-voltage shutdown
- Output voltage trim

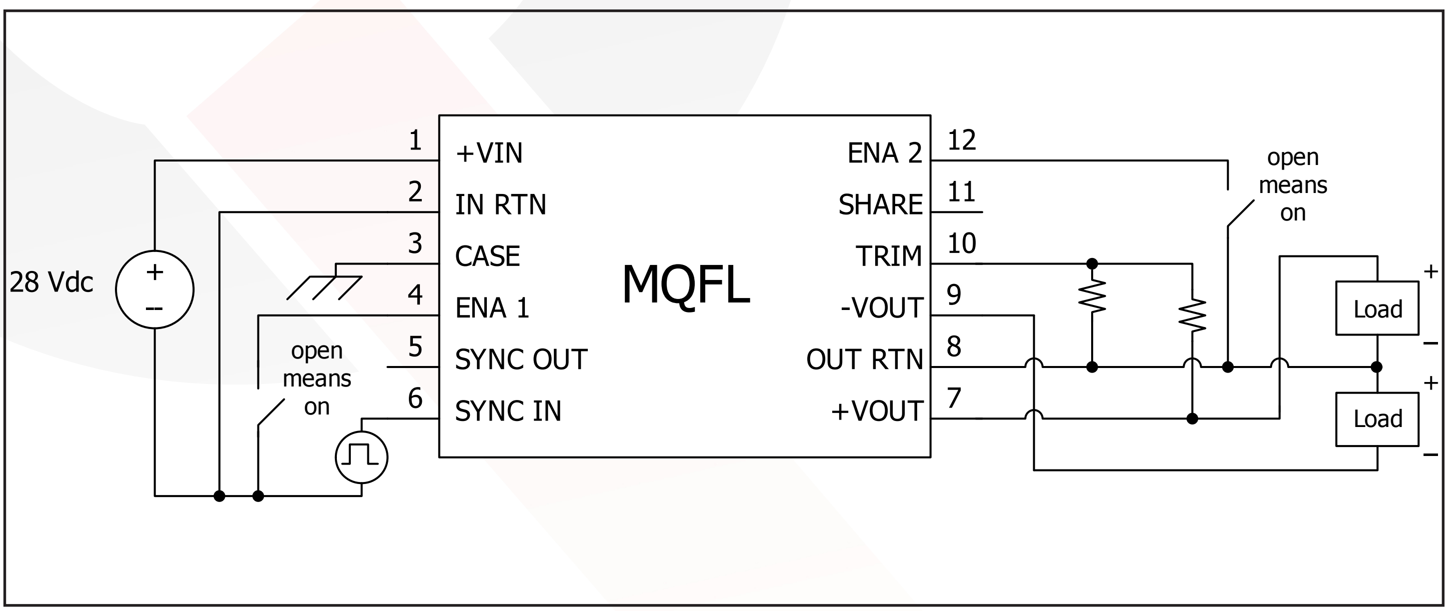
Specification Compliance

MQFL series converters (with MQME filter) are designed to meet:
- MIL-HDBK-704-8 (A through F)
- RTCA/DO-160 Section 16, 17, 18
- MIL-STD-1275 (B, D)
- DEF-STAN 61-5 (part 6)/(5, 6)
- MIL-STD-461 (C, D, E, F)
- RTCA/DO-160(E, F, G) Section 22

BLOCK DIAGRAM



TYPICAL CONNECTION DIAGRAM



MQFL-28-6R5D ELECTRICAL CHARACTERISTICS

Parameter Specifications subject to change without notice	Min.	Typ.	Max.	Units	Notes & Conditions Vin=28 Vdc ±5%, +Iout = -Iout = 9 A, CL=0 µF, free running (see Note 10) unless otherwise specified	Group A Subgroup (see Note 14)
ABSOLUTE MAXIMUM RATINGS						
Input Voltage						
Non-Operating			60	V		
Operating			60	V	See Note 1	
Reverse Bias (Tcase = 125 ºC)			-0.8	V		
Reverse Bias (Tcase = -55 ºC)			-1.2	V		
Isolation Voltage (I/O to case, I to O)						
Continuous	-500		500	V		
Transient (≤100 µs)	-800		800	V		
Operating Case Temperature	-55		125	°C	HB Grade Products, See Notes 2 & 16	
Storage Case Temperature	-65		135	°C		
Lead Temperature (20 s)			300	°C		
Voltage at ENA1, ENA2	-1.2		50	V		
INPUT CHARACTERISTICS						
Operating Input Voltage Range	16	28	40	V	Continuous	1, 2, 3
Operating Input Voltage Range	16	28	50	V	Transient, 1 s	
Input Under-Voltage Lockout					See Note 3	
Turn-On Voltage Threshold	14.75	15.50	16.00	V		1, 2, 3
Turn-Off Voltage Threshold	13.80	14.40	15.00	V		1, 2, 3
Lockout Voltage Hysteresis	0.5	1.1	1.8	V		
Input Over-Voltage Shutdown					See Note 3	
Turn-Off Voltage Threshold	54.0	56.8	60.0	V		
Turn-On Voltage Threshold	50.0	51.4	54.0	V		
Shutdown Voltage Hysteresis	2.0	5.3	8.0	V		
Input Filter Component Values (L\C)		2.0\24.6		µH\µF	Internal Values	
Maximum Input Current			9.5	A	Vin = 16 V; +Iout = -Iout = 9 A	See Note 5
No Load Input Current (operating)		110	160	mA		1, 2, 3
Disabled Input Current (ENA1)		2	5	mA		1, 2, 3
Disabled Input Current (ENA2)		25	50	mA		1, 2, 3
Input Terminal Current Ripple (peak to peak)		40	65	mA	Bandwidth = 100 kHz – 10 MHz; see Figure 20	1, 2, 3
OUTPUT CHARACTERISTICS						
Output Voltage Set Point (Tcase = 25 ºC)					See Note 12	
Positive Output	6.44	6.50	6.57	V		1
Negative Output	-6.57	-6.50	-6.44	V		1
Output Voltage Set Point Over Temperature					See Note 12	
Positive Output	6.40	6.50	6.60	V		2, 3
Negative Output	-6.60	-6.50	-6.40	V		2, 3
Output Voltage Line Regulation	-20	0	20	mV	See Note 12	1, 2, 3
Output Voltage Load Regulation	25	35	45	mV	+Vout@(+Iout=-Iout=0 A) - +Vout@(+Iout=-Iout=9 A); See Note 12	1, 2, 3
Total Output Voltage Range	6.37	6.50	6.63	V	See Note 12	1, 2, 3
Output Voltage Cross Regulation	100	200	350	mV	-Vout @ (+Iout = -Iout =3.6 A) - -Vout @ (+Iout = 14.4 A, -Iout = 3.6 A); See Notes 11, 12	1, 2, 3
Output Voltage Ripple and Noise Peak to Peak		20	80	mV	Bandwidth = 100 kHz - 10 MHz; C_L= 11 µF on both outputs	1, 2, 3
Operating Output Current Range	0		18	A	(+Iout) + (-Iout)	1, 2, 3
Single Output Operating Current Range	0		14.4	A	Maximum +Iout or -Iout	1, 2, 3
Operating Output Power Range	0		117	W	Total on both outputs	1, 2, 3
Output DC Current-Limit Inception	19	22	25	A	+Iout + -Iout; +Iout - -Iout, See Note 4	1, 2, 3
Short Circuit Output Current	21	24	26	A	+Vout ≤ 1.2 V	See Note 5
Back-Drive Current Limit while Enabled		6		A		1, 2, 3
Back-Drive Current Limit while Disabled		10	50	mA		1, 2, 3
Maximum Output Capacitance			10000	µF	Total on both outputs; See Note 5	See Note 5
DYNAMIC CHARACTERISTICS						
Output Voltage Deviation Load Transient					See Note 6	
For a Pos. Step Change in Load Current	-450	-350		mV	Total Iout Step = 9 A ↔ 18 A, 1.8 A ↔ 9 A; CL= 11 µF on both outputs	4, 5, 6
For a Neg. Step Change in Load Current		350	450	mV	"	4, 5, 6
Settling Time (either case)		100	300	µs	See Note 7	
Output Voltage Deviation Line Transient					See Note 8	
For a Pos. Step Change in Line Voltage	-500		500	mV	Vin step = 16 V ↔ 50 V; C_L= 11 µF on both outputs	
For a Neg. Step Change in Line Voltage	-500		500	mV		
Settling Time (either case)		250	500	µs	See Note 7	
Turn-On Transient						
Output Voltage Rise Time		6	10	ms	+Vout = 0.65 V -> 5.85 V	4, 5, 6
Output Voltage Overshoot		0	2	%		See Note 5
Turn-On Delay, Rising Vin		5.5	8.0	ms	ENA1, ENA2 = 5 V; See Note 9	4, 5, 6
Turn-On Delay, Rising ENA1		3.0	6.0	ms	ENA2 = 5 V	4, 5, 6
Turn-On Delay, Rising ENA2		1.5	3.0	ms	ENA1 = 5 V	4, 5, 6

MQFL-28-6R5D ELECTRICAL CHARACTERISTICS (Continued)

Parameter Specifications subject to change without notice	Min.	Typ.	Max.	Units	Notes & Conditions Vin=28 Vdc ±5%, +Iout = -Iout = 9 A, CL=0 µF, free running (see Note 10) unless otherwise specified	Group A Subgroup (see Note 14)
EFFICIENCY						
Iout = 18 A (16 Vin)	85	89		%		
Iout = 9 A (16 Vin)	88	92		%		
Iout = 18 A (28 Vin)	85	90		%		1, 2, 3
Iout = 9 A (28 Vin)	88	91		%		
Iout = 18 A (40 Vin)	84	88		%		
Iout = 9 A (40 Vin)	87	90		%		
Load Fault Power Dissipation		18	32	W	Iout at current limit inception point; See Note 4	1
Short Circuit Power Dissipation		20	33	W	+Vout ≤ + 1.2 V; -Vout ≥ -1.2 V	1
ISOLATION CHARACTERISTICS						
Isolation Voltage					Dielectric strength	
Input RTN to Output RTN	500			V		1
Any Input Pin to Case	500			V		1
Any Output Pin to Case	500			V		1
Isolation Resistance (input rtn to output rtn)	100			MΩ		1
Isolation Resistance (any pin to case)	100			MΩ		1
Isolation Capacitance (input rtn to output rtn)		44		nF		1
FEATURE CHARACTERISTICS						
Switching Frequency (free running)	500	550	600	kHz		1, 2, 3
Synchronization Input						
Frequency Range	500		700	kHz		1, 2, 3
Logic Level High	2		10	V		1, 2, 3
Logic Level Low	-0.5		0.8	V		1, 2, 3
Duty Cycle	20		80	%		See Note 5
Synchronization Output						
Pull Down Current	20			mA	VSYNC OUT = 0.8 V	See Note 5
Duty Cycle	25		75	%	Output connected to SYNC IN of another MQFL unit	See Note 5
Enable Control (ENA1 and ENA2)						
Off-State Voltage			0.8	V		1, 2, 3
Module Off Pulldown Current	80			µA	Current drain required to ensure module is off	See Note 5
On-State Voltage	2			V		1, 2, 3
Module On Pin Leakage Current			20	µA	Maximum current draw from pin allowed with module still on	See Note 5
Pull-Up Voltage	3.2	4.0	4.5	V	See Figure A	1, 2, 3
Output Voltage Trim Range	-0.7		0.5	V	(+Vout) - 6.5 V; See Figure E	See Note 5
RELIABILITY CHARACTERISTICS						
Calculated MTBF (MIL-STD-217F2)						
GB @ Tcase = 70 ºC		2800		10^3 Hrs.		
AIF @ Tcase = 70 ºC		420		10^3 Hrs.		
WEIGHT CHARACTERISTICS						
Device Weight		79		g		

Electrical Characteristics Notes

1. Converter will undergo input over-voltage shutdown.
2. Derate output power to 50% of rated power at Tcase = 135 ºC. 135 ºC is above specified operating range.
3. High or low state of input voltage must persist for about 200 µs to be acted on by the lockout or shutdown circuitry.
4. Current limit inception is defined as the point where the output voltage has dropped to 90% of its nominal value.
5. Parameter not tested but guaranteed to the limit specified.
6. Load current transition time ≥ 10 µs.
7. Settling time measured from start of transient to the point where the output voltage has returned to ±1% of its final value.
8. Line voltage transition time ≥ 100 µs.
9. Input voltage rise time ≤ 250 µs.
10. Operating the converter at a synchronization frequency above the free running frequency will slightly reduce the converter's efficiency and may also cause a slight reduction in the maximum output current/power available. For more information consult the factory.
11. The regulation stage operates to control the positive output. The Negative output displays cross regulation.
12. All +Vout and -Vout voltage measurements are made with Kelvin probes on the output leads.
13. SHARE pin outputs a power failure warning pulse during a fault condition. See Current Share section.
14. Only the ES and HB grade products are tested at three temperatures. The C- grade products are tested at one temperature. Please refer to the Construction and Environmental Stress Screening Options table for details.
15. These derating curves apply for the ES and HB grade products. The C- grade product has a maximum case temperature of 70 °C and a maximum junction temperature rise of 20 °C at full load.
16. The specified operating case temperature for ES grade products is -45 ºC to 100 ºC. The specified operating case temperature for C- grade products is 0 ºC to 70 ºC.

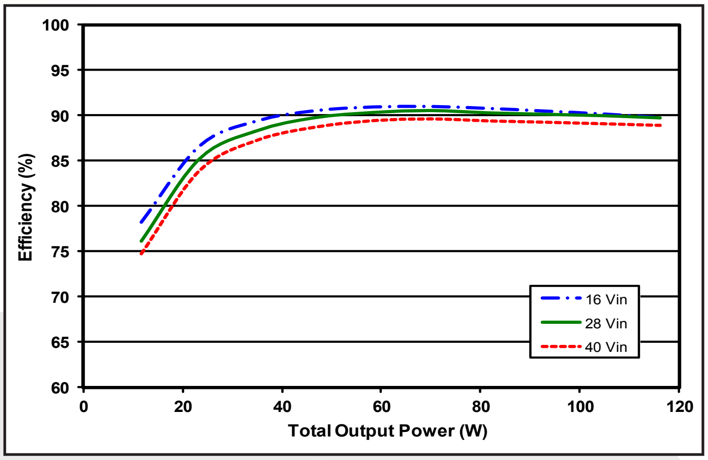


Figure 1: Efficiency vs. output power, from zero load to full load with equal load on the +6.5 V and -6.5 V outputs at minimum, nominal, and maximum input voltage at 25 °C.

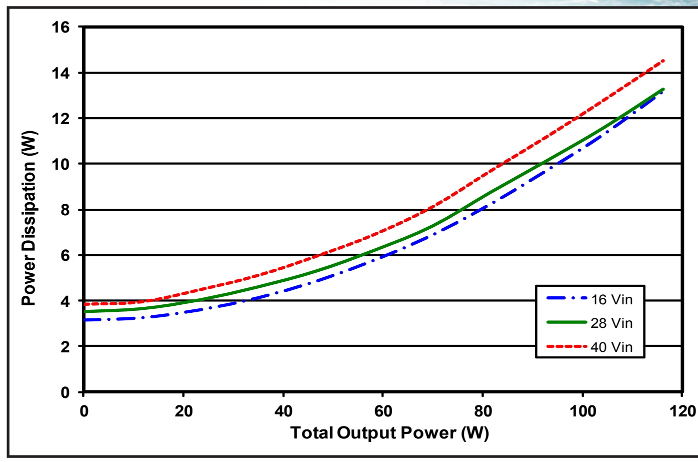


Figure 2: Power dissipation vs. output power, from zero load to full load with equal load on the +6.5 V and -6.5 V outputs at minimum, nominal, and maximum input voltage at 25 °C.

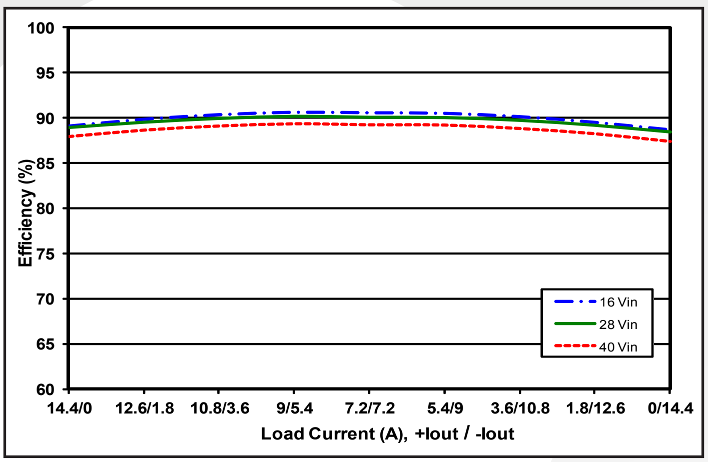


Figure 3: Efficiency vs. output current, with total output current fixed at 80% load (93.6 W) and loads split as shown between the +6.5 V and -6.5 V outputs at minimum, nominal, and maximum input voltage at 25 °C.

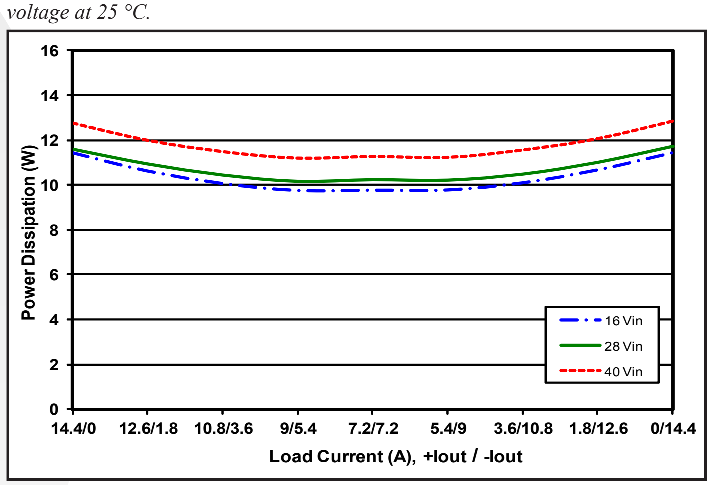


Figure 4: Power dissipation vs. output current, with total output current fixed at 80% load (93.6 W) and loads split as shown between the +6.5 V and -6.5 V outputs at minimum, nominal, and max input voltage at 25 °C.

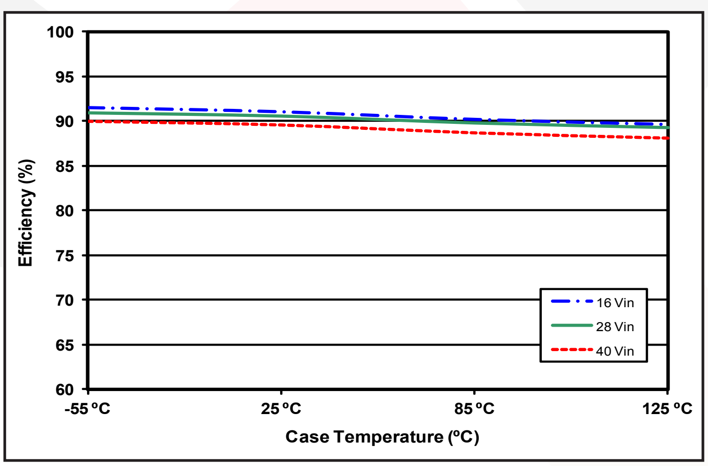


Figure 5: Efficiency at 60% load (5.4 A load on +6.5 V and 5.4 A load on -6.5 V) versus case temperature for Vin = 16 V, 28 V, and 40 V.

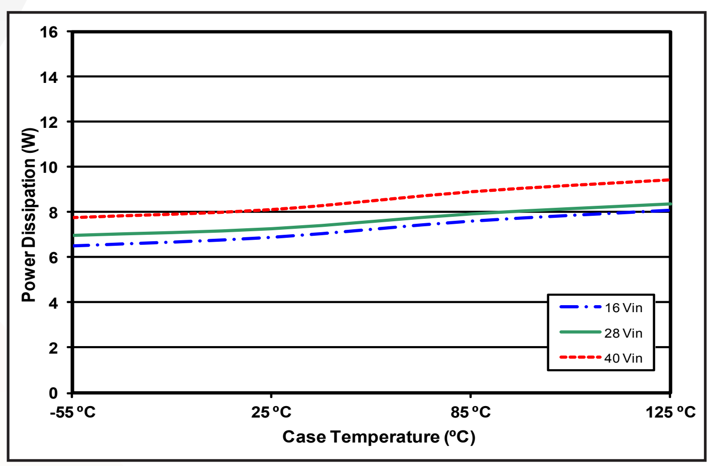


Figure 6: Power dissipation at 60% load (5.4 A load on +6.5 V and 5.4 A load on -6.5 V) versus case temperature for Vin =16 V, 28 V, and 40 V.

Technical Figures

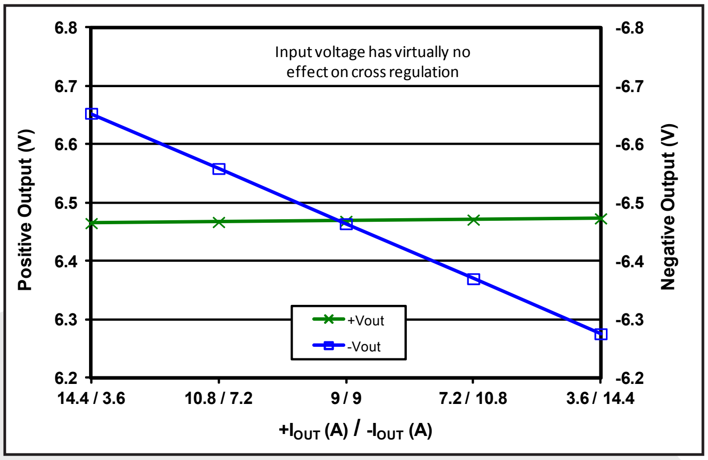


Figure 7: Load regulation vs. load current with power fixed at full load (117 W) and load currents split as shown between the +6.5 V and -6.5 V outputs, at nominal input voltage and Tcase = 25 ºC.

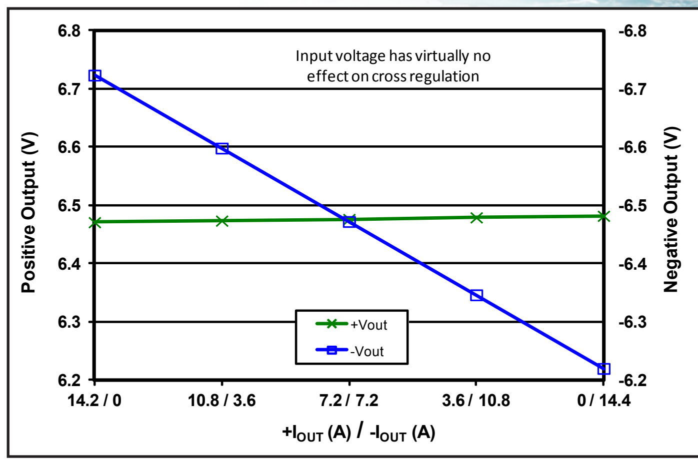


Figure 8: Load regulation vs. load current with power fixed at 80% load (93.6 W) and load currents split as shown between the +6.5 V and -6.5 V outputs, at nominal input voltage and Tcase = 25 ºC.

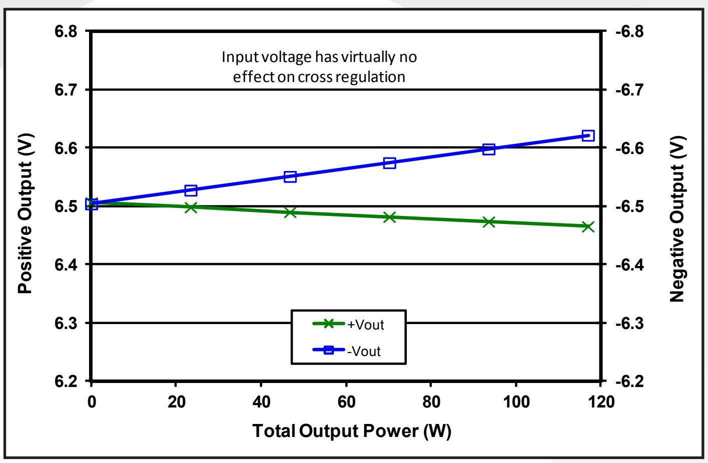


Figure 9: Load regulation vs. total output power from zero to to full load where +Iout equals three times -Iout at nominal input voltage and Tcase = 25 ºC.

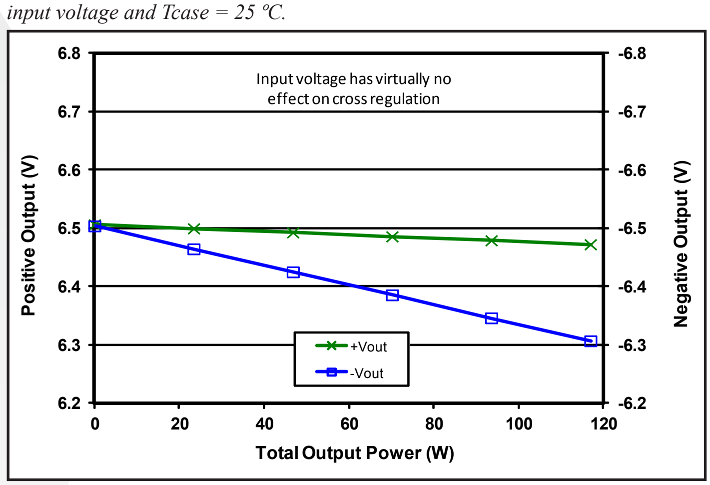


Figure 10: Load regulation vs. total output power from zero to to full load where -Iout equals three times +Iout at nominal input voltage and Tcase = 25 ºC.

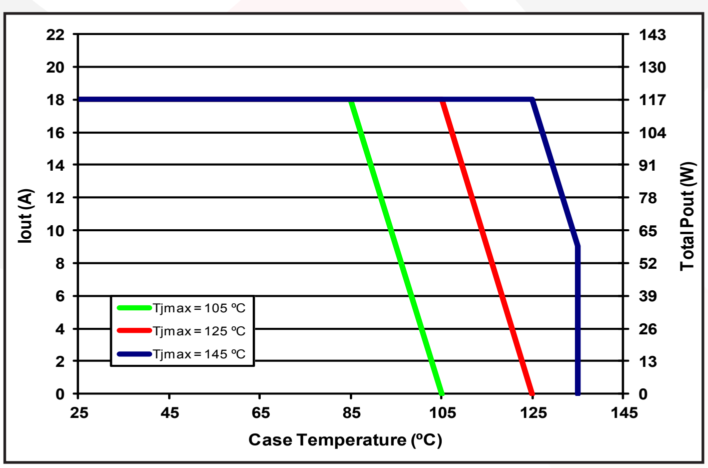


Figure 11: Total Output Current / Total Output Power derating curve as a function of Tcase and the maximum desired power MOSFET junction temperature at Vin = 28 V (see Note 15).

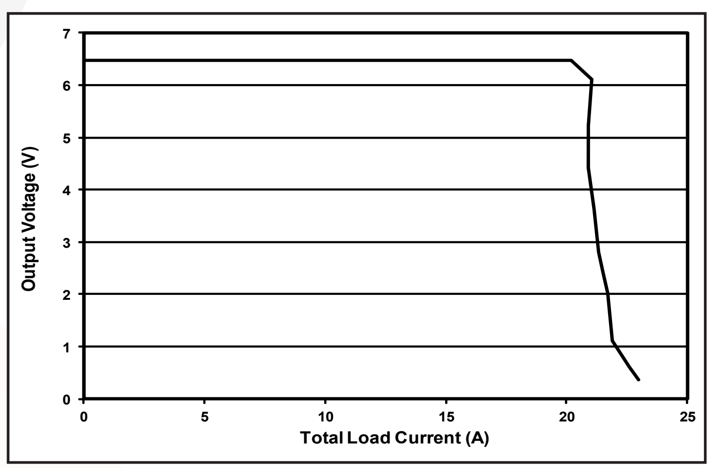


Figure 12: Positive output voltage vs. total load current, evenly split, showing typical current limit curves at Vin = 28 V.

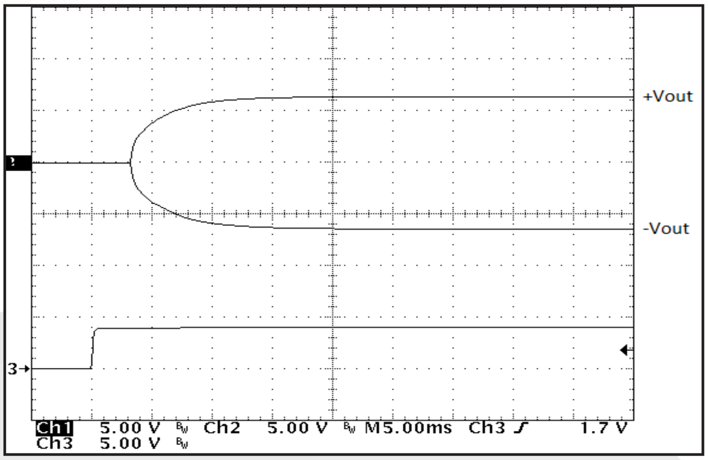


Figure 13: Turn-on transient at full rated load current (resistive load) (5 ms/div). Input voltage pre-applied. Ch 1: +Vout (5 V/div); Ch 2: -Vout (5 V/div); Ch 3: Enable1 input (5 V/div).

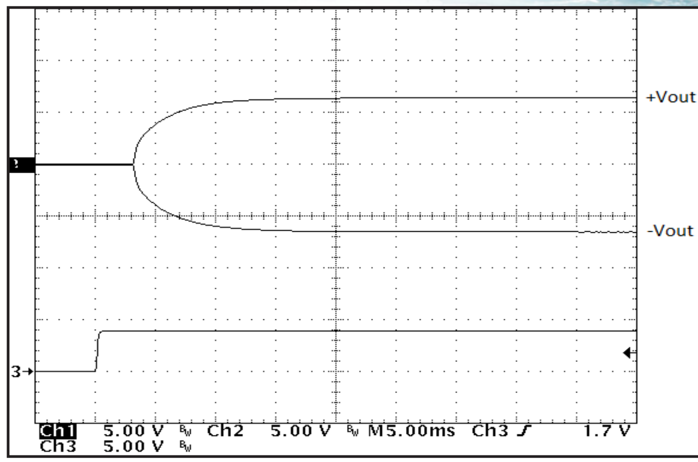


Figure 14: Turn-on transient at zero load current (5 ms/div). Input voltage pre-applied. Ch 1: +Vout (5 V/div); Ch 2: -Vout (5 V/div); Ch 3: Enable1 input (5 V/div).

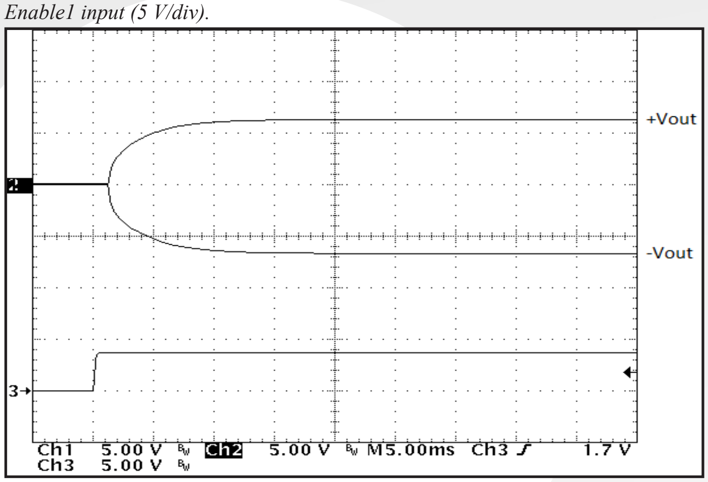


Figure 15: Turn-on transient at full rated load current (resistive load) (5 ms/div). Input voltage pre-applied. Ch 1: +Vout (5 V/div); Ch 2: -Vout (5 V/div); Ch 3: Enable2 input (5 V/div).

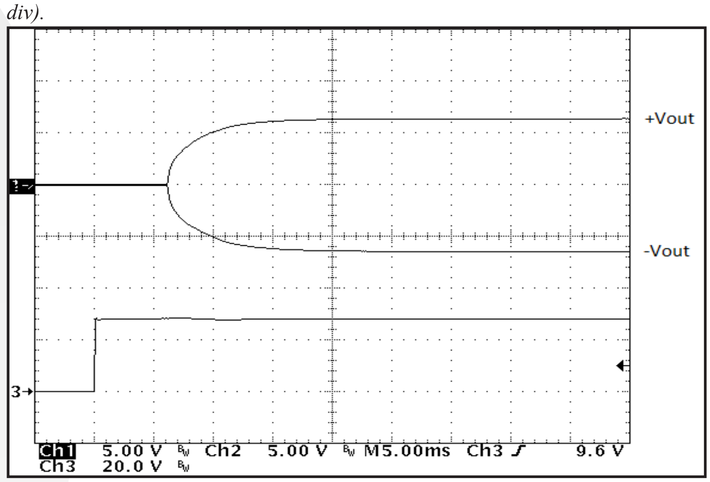


Figure 16: Turn-on transient at full load, after application of input voltage (ENA 1 and ENA 2 logic high) (5 ms/div). Ch 1: +Vout (5 V/ div); Ch 2: -Vout (5 V/div); Ch 3: Vin (10 V/div).

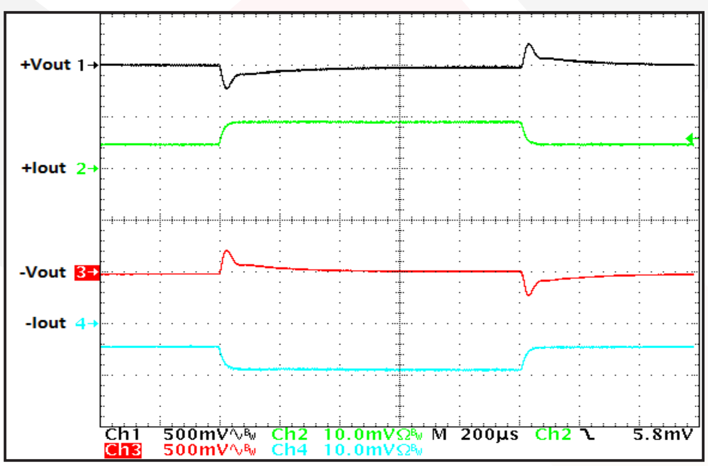


Figure 17: Output voltage response to step-change in total load current (50%-100%-50%) of total Iout (max) split 50%/50%. Load cap: 1 µF ceramic cap and 10 µF, 100 mΩ ESR tantalum cap. Ch 1: +Vout (500 mV/div); Ch 2: +Iout (10 A/div); Ch 3: -Vout (500 mV/div); Ch 4: -Iout (10 A/div).

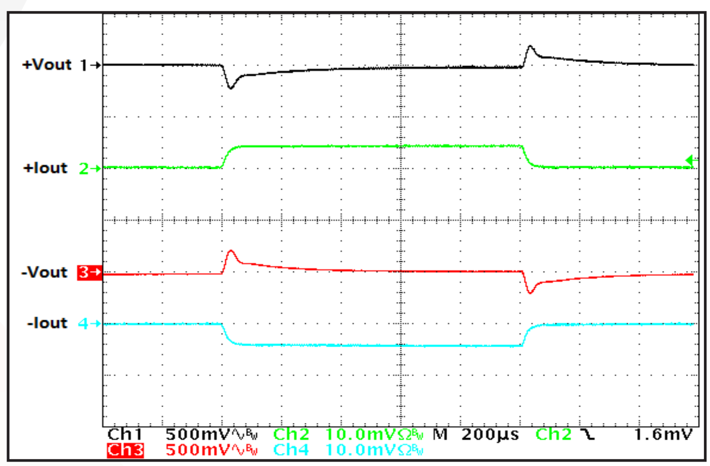


Figure 18: Output voltage response to step-change in total load current (0%-50%-0%) of total Iout (max) split 50%/50%. Load cap: 1 µF ceramic cap and 10 µF, 100 mΩ ESR tantalum cap. Ch 1: +Vout (500 mV/div); Ch 2: +Iout (10 A/div); Ch 3: -Vout (500 mV/div); Ch 4: -Iout (10 A/div).

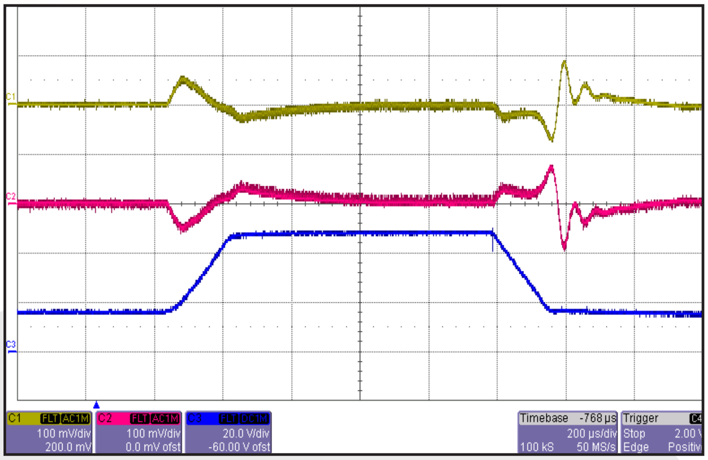


Figure 19: Output voltage response to step-change in input voltage (16 V - 50 V - 16 V). Load cap: 10 µF, 100 mΩ ESR tantalum cap and 1 µF ceramic cap. Ch 1: +Vout (100 mV/div); Ch 2: -Vout (100 mV/ div); Ch 3: Vin (20 V/div).

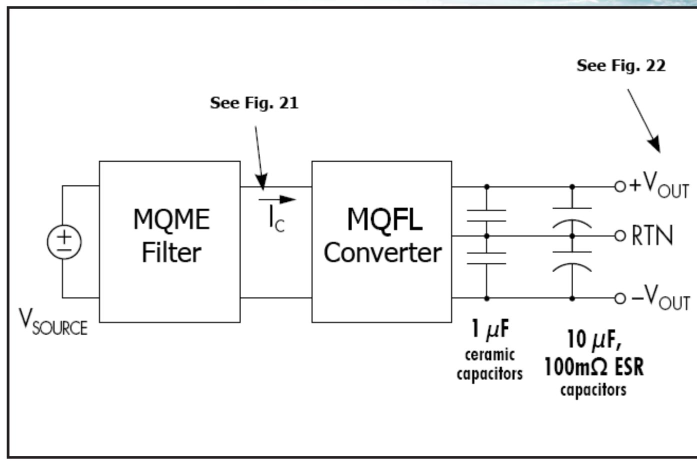


Figure 20: Test set-up diagram showing measurement points for Input Terminal Ripple Current (Figure 21) and Output Voltage Ripple (Figure 22).

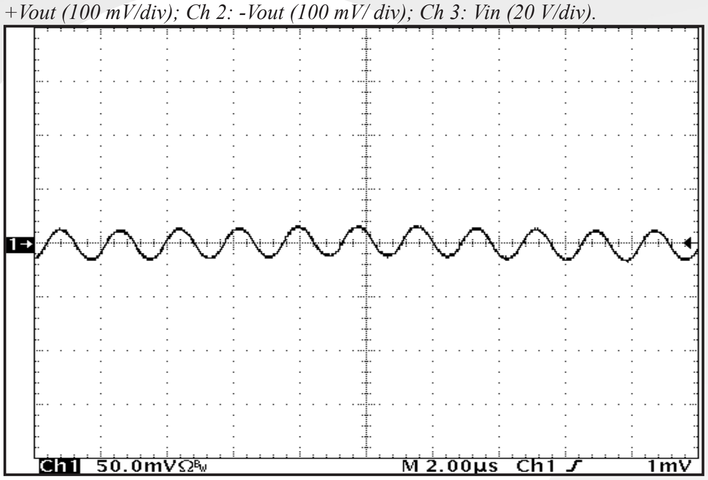


Figure 21: Input terminal current ripple, ic, at full rated output current and nominal input voltage with SynQor MQ filter module (50 mA/div). Bandwidth: 20 MHz. See Figure 20.

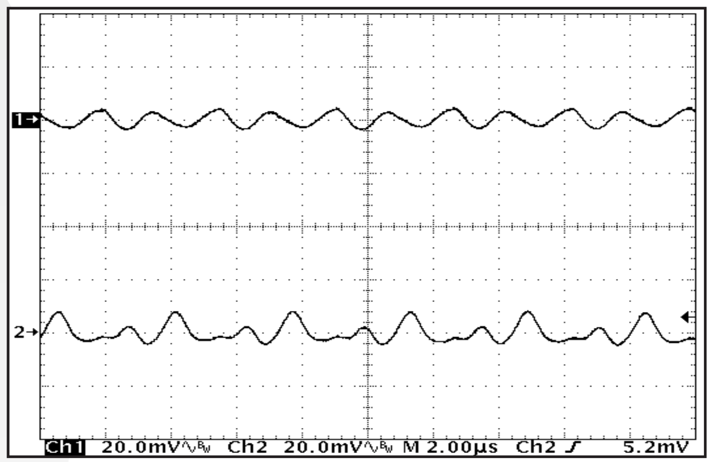


Figure 22: Output voltage ripple, +Vout (Ch 1) and -Vout (Ch 2), at nominal input voltage and full load current evenly split (20 mV/ div). Load capacitance: 1 µF ceramic cap and 10 µF tantalum cap. Bandwidth: 10 MHz. See Figure 20.

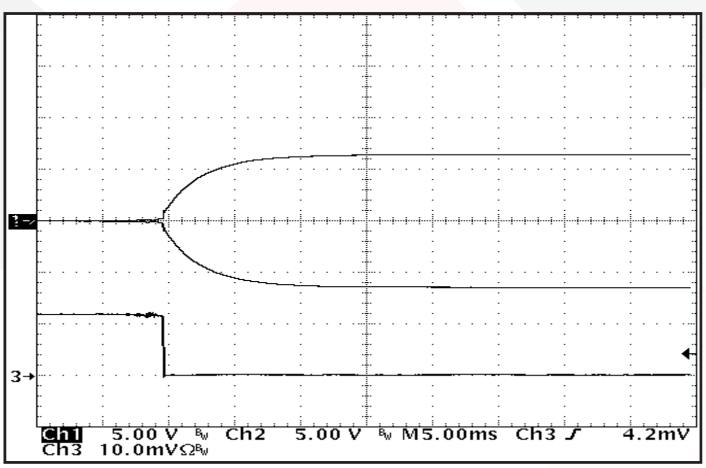


Figure 23: Rise of output voltage after the removal of a short circuit across the positive output terminals. Ch 1: +Vout (5 V/div); Ch 2: -Vout (5 V/div); Ch 3: +Iout (10 A/div).

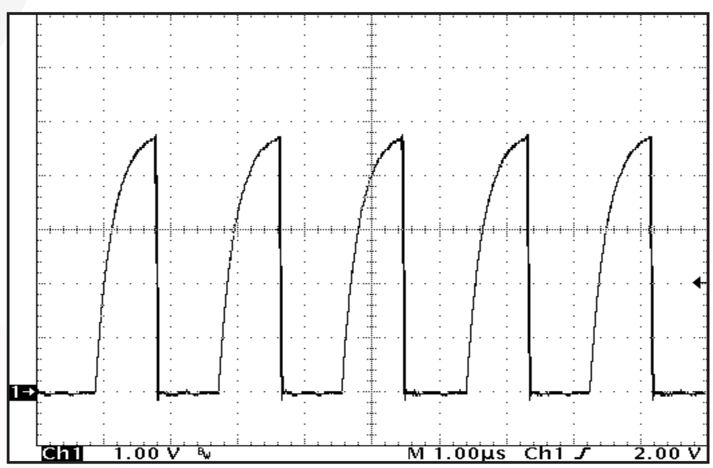


Figure 24:SYNC OUT vs. time, driving SYNC IN of a second SynQor MQFL converter.

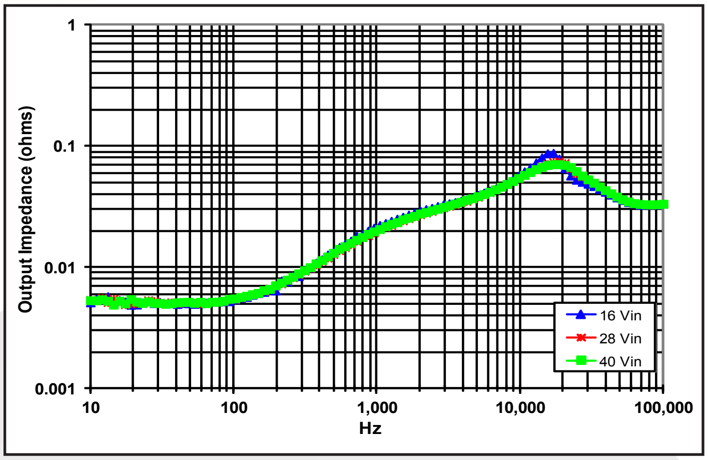


Figure 25: Magnitude of incremental output impedance of +6.5 V output (+Zout = +vout /+iout) for minimum, nominal, and maximum input voltage at full rated power.

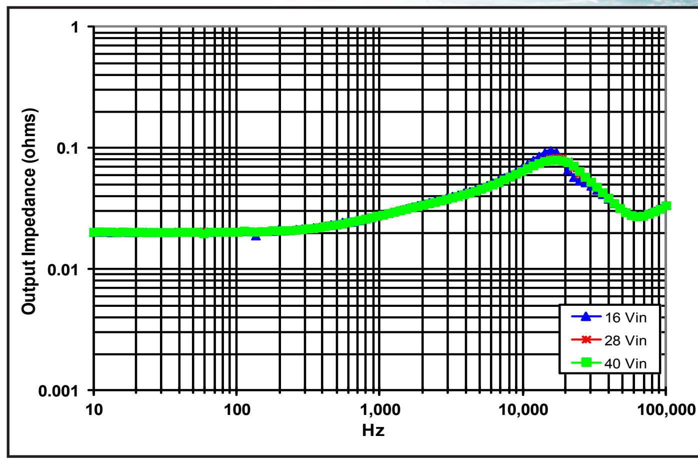


Figure 26: Magnitude of incremental output impedance of -6.5 V output (-Zout = -vout /-iout) for minimum, nominal, and maximum input voltage at full rated power.

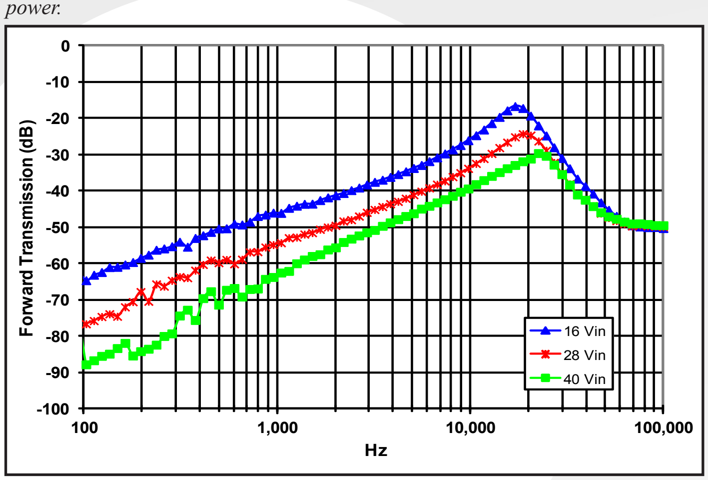


Figure 27: Magnitude of incremental forward transmission of +6.5 V output (+FT = +vout /vin) for minimum, nominal, and maximum input voltage at full rated power.

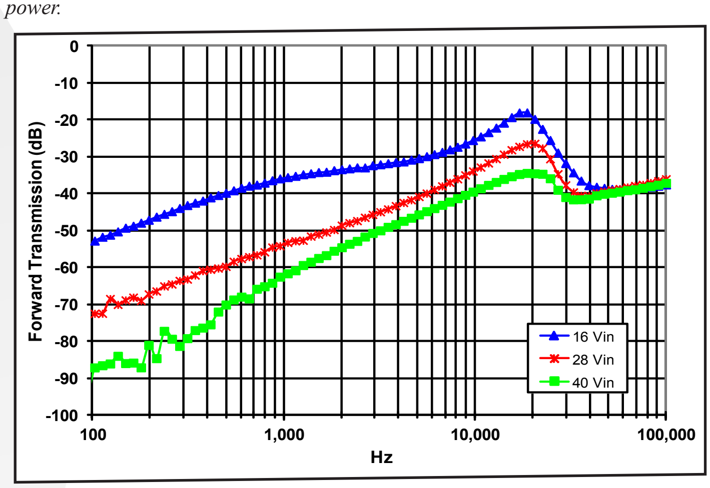


Figure 28: Magnitude of incremental forward transmission of -6.5 V output (-FT = -vout /vin) for minimum, nominal, and maximum input voltage at full rated power.

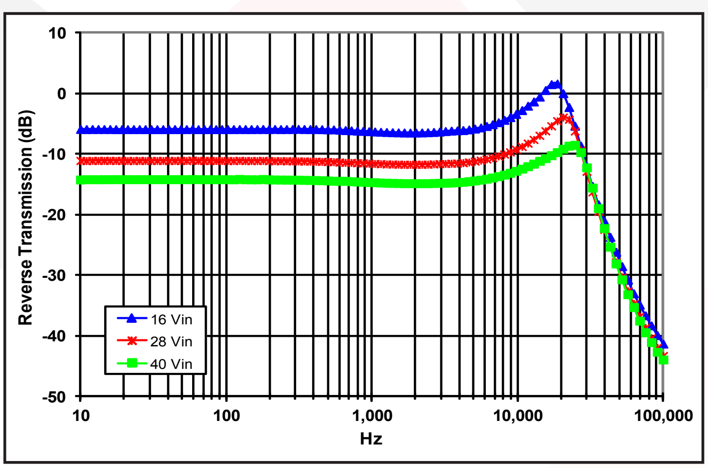


Figure 29: Magnitude of incremental reverse transmission from +6.5 V output (+RT = iin /+iout) for minimum, nominal, and maximum input voltage at full rated power.

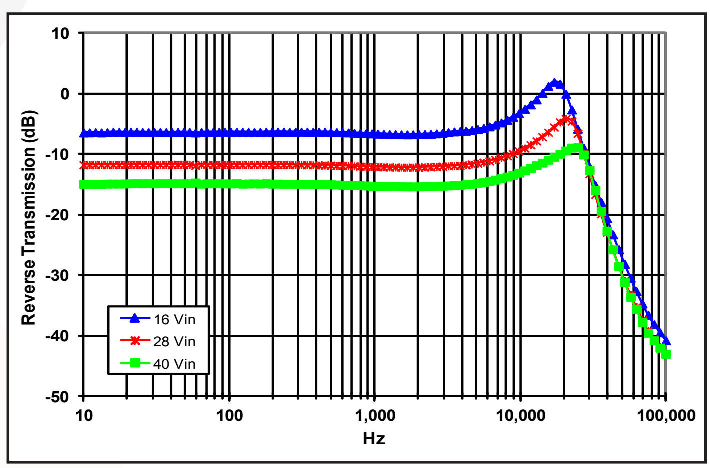


Figure 30: Magnitude of incremental reverse transmission from -6.5 V output (-RT = iin /-iout) for minimum, nominal, and maximum input voltage at full rated power.

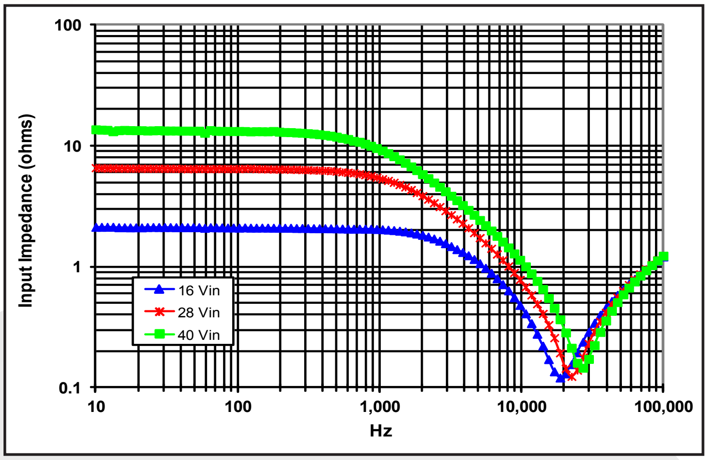


Figure 31: Magnitude of incremental input impedance (Zin = vin/iin) for minimum, nominal, and maximum input voltage at full rated power with 50% / 50% split.

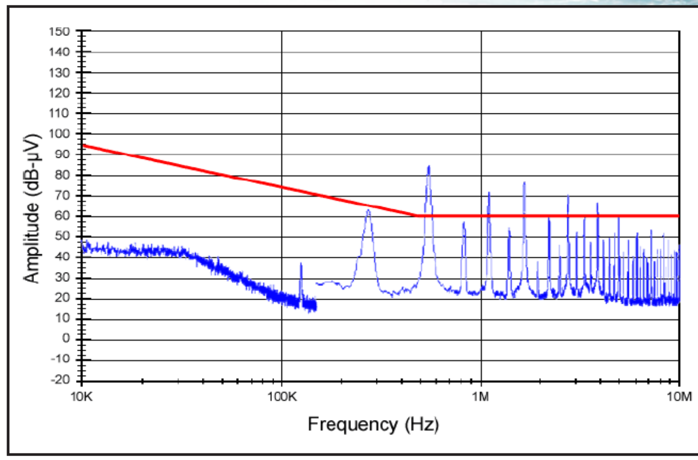


Figure 32: High frequency conducted emissions of standalone MQFL-28-05S, 5 Vout module at 120 W output, as measured with Method CE102. Limit line shown is the 'Basic Curve' for all applications with a 28 V source.

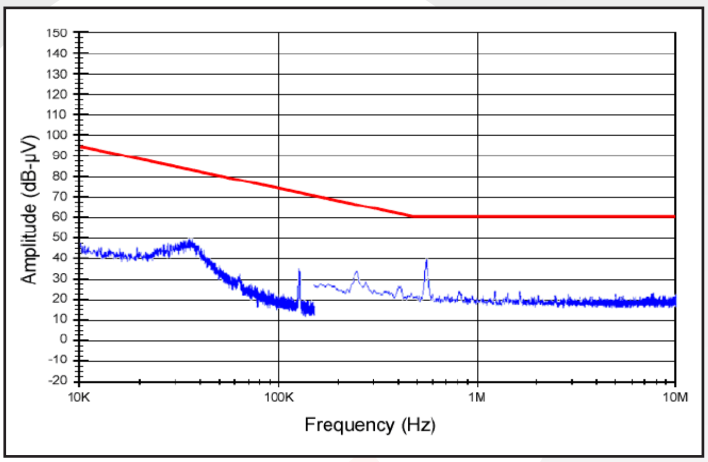


Figure 33: High frequency conducted emissions of MQFL-28-05S, 5 Vout module at 120 W output with MQFL-28-P filter, as measured with Method CE102. Limit line shown is the 'Basic Curve' for allapplications with a 28 V source.

BASIC OPERATION AND FEATURES

The MQFL DC-DC converter uses a two-stage power conversion topology. The first, or regulation, stage is a buck-converter that keeps the output voltage constant over variations in line, load, and temperature. The second, or isolation, stage uses transformers to provide the functions of input/output isolation and voltage transformation to achieve the output voltage required.

In the dual output converter there are two secondary windings in the transformer of the isolation stage, one for each output. There is only one regulation stage, however, and it is used to control the positive output. The negative output therefore displays "Cross-Regulation", meaning that its output voltage depends on how much current is drawn from each output.

Both the positive and the negative outputs share a common OUTPUT RETURN pin.

Both the regulation and the isolation stages switch at a fixed frequency for predictable EMI performance. The isolation stage switches at one half the frequency of the regulation stage, but due to the push-pull nature of this stage it creates a ripple at double its switching frequency. As a result, both the input and the output of the converter have a fundamental ripple frequency of about 550 kHz in the free-running mode.

Rectification of the isolation stage's output is accomplished with synchronous rectifiers. These devices, which are MOSFETs with a very low resistance, dissipate far less energy than would Schottky diodes. This is the primary reason why the MQFL converters have such high efficiency, particularly at low output voltages.

Besides improving efficiency, the synchronous rectifiers permit operation down to zero load current. There is no longer a need for a minimum load, as is typical for converters that use diodes for rectification. The synchronous rectifiers actually permit a negative load current to flow back into the converter's output terminals if the load is a source of short or long term energy. The MQFL converters employ a "back-drive current limit" to keep this negative output terminal current small.

There is a control circuit on both the input and output sides of the MQFL converter that determines the conduction state of the power switches. These circuits communicate with each other across the isolation barrier through a magnetically coupled device. No opto-isolators are used.

A separate bias supply provides power to both the input and output control circuits. Among other things, this bias supply permits the converter to operate indefinitely into a short circuit and to avoid a hiccup mode, even under a tough start-up condition.

An input under-voltage lockout feature with hysteresis is provided, as well as an input over-voltage shutdown. There is also an output current limit that is nearly constant as the load impedance decreases to a short circuit (i.e., there is not fold-back or fold-forward characteristic to the output current under this condition). When a load fault is removed, the output voltage rises exponentially to its nominal value without an overshoot.

The MQFL converter's control circuit does not implement an output over-voltage limit or an over-temperature shutdown.

The following sections describe the use and operation of additional control features provided by the MQFL converter.

CONTROL FEATURES

ENABLE: The MQFL converter has two enable pins. Both must have a logic high level for the converter to be enabled. A logic low on either pin will inhibit the converter.

The ENA1 pin (pin 4) is referenced with respect to the converter's input return (pin 2). The ENA2 pin (pin 12) is referenced with respect to the converter's output return (pin 8). This permits the converter to be inhibited from either the input or the output side.

Regardless of which pin is used to inhibit the converter, the regulation and the isolation stages are turned off. However, when the converter is inhibited through the ENA1 pin, the bias supply is also turned off, whereas this supply remains on when the converter is inhibited through the ENA2 pin. A higher input standby current therefore results in the latter case.

Both enable pins are internally pulled high so that an open connection on both pins will enable the converter. Figure A shows the equivalent circuit looking into either enable pins. It is TTL compatible.

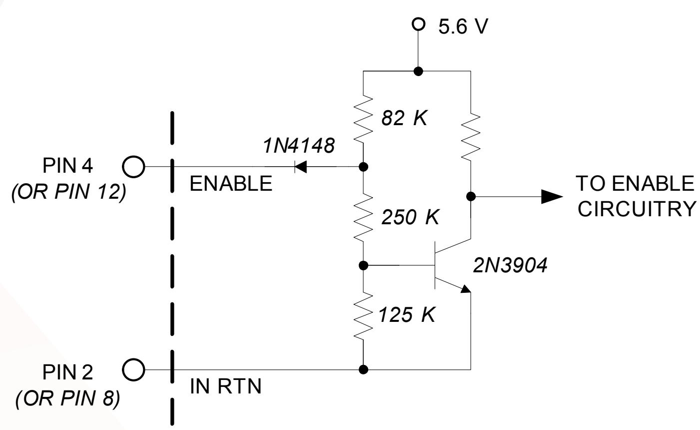


Figure A: *Circuit diagram shown for reference only, actual circuit components may differ from values shown for equivalent circuit.*

SYNCHRONIZATION: The MQFL converter's switching frequency can be synchronized to an external frequency source that is in the 500 kHz to 700 kHz range. A pulse train at the desired frequency should be applied to the SYNC IN pin (pin 6) with respect to the INPUT RETURN (pin 2). This pulse train should have a duty cycle in the 20% to 80% range. Its low value should be below 0.8 V to be guaranteed to be interpreted as a logic low, and its high value should be above 2.0 V to be guaranteed to be interpreted as a logic high. The transition time between the two states should be less than 300 ns.

If the MQFL converter is not to be synchronized, the SYNC IN pin should be left open circuit. The converter will then operate in its free-running mode at a frequency of approximately 550 kHz.

If, due to a fault, the SYNC IN pin is held in either a logic low or logic high state continuously, the MQFL converter will revert to its free-running frequency.

The MQFL converter also has a SYNC OUT pin (pin 5). This output can be used to drive the SYNC IN pins of as many as ten (10) other MQFL converters. The pulse train coming out of SYNC OUT has a duty cycle of 50% and a frequency that matches the switching frequency of the converter with which it is associated. This frequency is either the free-running frequency if there is no synchronization signal at the SYNC IN pin, or the synchronization frequency if there is.

The SYNC OUT signal is available only when the DC input voltage is above approximately 12 V and when the converter is not inhibited through the ENA1 pin. An inhibit through the ENA2 pin will not turn the SYNC OUT signal off.

NOTE: An MQFL converter that has its SYNC IN pin driven by the SYNC OUT pin of a second MQFL converter will have its start of its switching cycle delayed approximately 180 degrees relative to that of the second converter.

Figure B shows the equivalent circuit looking into the SYNC IN pin. Figure C shows the equivalent circuit looking into the SYNC OUT pin.

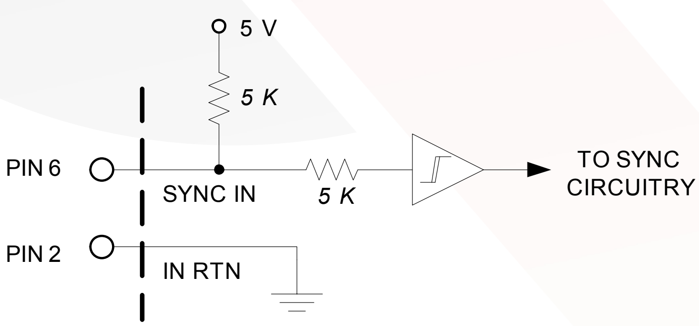


Figure B: *Equivalent circuit looking into the SYNC IN pin with respect to the IN RTN (input return) pin.*

CURRENT SHARE: When several MQFL converters are placed in parallel to achieve either a higher total load power or N+1 redundancy, their SHARE pins (pin 11) should be connected together. The voltage on this common SHARE node represents the average current delivered by all of the paralleled converters. Each converter monitors this average value and adjusts itself so that its output current closely matches that of the average.

Since the SHARE pin is monitored with respect to the OUTPUT RETURN (pin 8) by each converter, it is important to connect all of the converters' OUTPUT RETURN pins together through a low DC and AC impedance. When this is done correctly, the converters will deliver their appropriate fraction of the total load current to within +/- 10% at full rated load.

Whether or not converters are paralleled, the voltage at the SHARE pin could be used to monitor the approximate average current delivered by the converter(s). A nominal voltage of 1.0 V represents zero current and a nominal voltage of 2.2 V represents the maximum rated current, with a linear relationship in between. The internal source resistance of a converter's SHARE pin signal is 2.5 kW. During an input voltage fault or primary disable event, the SHARE pin outputs a power failure warning pulse. The SHARE pin will go to 3 V for approximately 14 ms as the output voltage falls.

NOTE: Converters operating from separate input filters with reverse polarity protection (such as the MQME-28-T filter) with their outputs connected in parallel may exhibit hiccup operation at light loads. Consult factory for details.

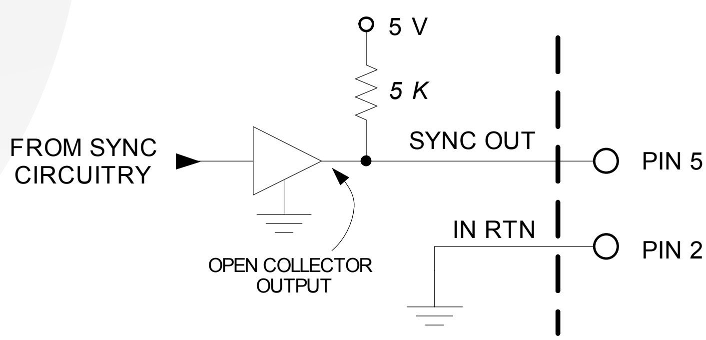


Figure C: *Equivalent circuit looking into SYNC OUT pin with respect to the IN RTN (input return) pin.*

OUTPUT VOLTAGE TRIM: If desired, it is possible to increase the MQFL dual converter's output voltage above its nominal value. To increase the output voltage a resistor, Rup, should be connected between the TRIM pin (pin 10) and the OUTPUT RETURN pin (pin 8), as shown in Figure D. The value of this resistor should be determined according to the following equation:

$$\text{Rup} = 10 \times \left(\frac{\text{Vnom} - 2.5}{\text{Vout} - \text{Vnom}} - 2 \times \text{Vnom} + 5 \right)$$

where:
Vnom = the converter's nominal output voltage,
Vout = the desired output voltage (greater than Vnom), and
Rup is in kiloOhms (kΩ).

The maximum value of output voltage that can be achieved is 0.5 V above the nominal output.

To decrease the output voltage a resistor, Rdown, should be connected between the TRIM pin and the POSITIVE OUTPUT pin (pin 7), as shown in Figure D. The value of this resistor should be determined according to the following equation:

$$\text{Rdown} = 10 \times \left[\frac{\text{Vnom}}{2.5} - 1 \right] \times \left[\frac{\text{Vout} - 2.5}{\text{Vnom} - \text{Vout}} - 5 \right]$$

where:
Vnom = the converter's nominal output voltage,
Vout = the desired output voltage (less than Vnom), and
Rdown is in kiloOhms (kΩ).

As the output voltage is trimmed up, it produces a greater voltage stress on the converter's internal components and may cause the converter to fail to deliver the desired output voltage at the low end of the input voltage range at the higher end of the load current and temperature range. Please consult the factory for details.

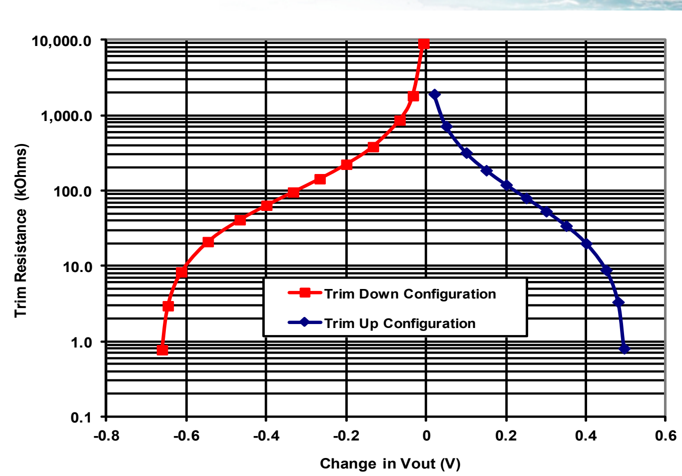


Figure E: Output Voltage Trim Graph

INPUT UNDER-VOLTAGE LOCKOUT: The MQFL converter has an under-voltage lockout feature that ensures the converter will be off if the input voltage is too low. The threshold of input voltage at which the converter will turn on is higher that the threshold at which it will turn off. In addition, the MQFL converter will not respond to a state of the input voltage unless it has remained in that state for more than about 200 μs. This hysteresis and the delay ensure proper operation when the source impedance is high or in a noisy environment.

INPUT OVER-VOLTAGE SHUTDOWN: The MQFL converter also has an over-voltage feature that ensures the converter will be off if the input voltage is too high. It also has a hysteresis and time delay to ensure proper operation.

SHUT DOWN: The MQFL converter will shut down in response to only four conditions: ENA1 input low, ENA2 input low, VIN input below under-voltage lockout threshold, or VIN input above over-voltage shutdown threshold. Following a shutdown event, there is a startup inhibit delay which will

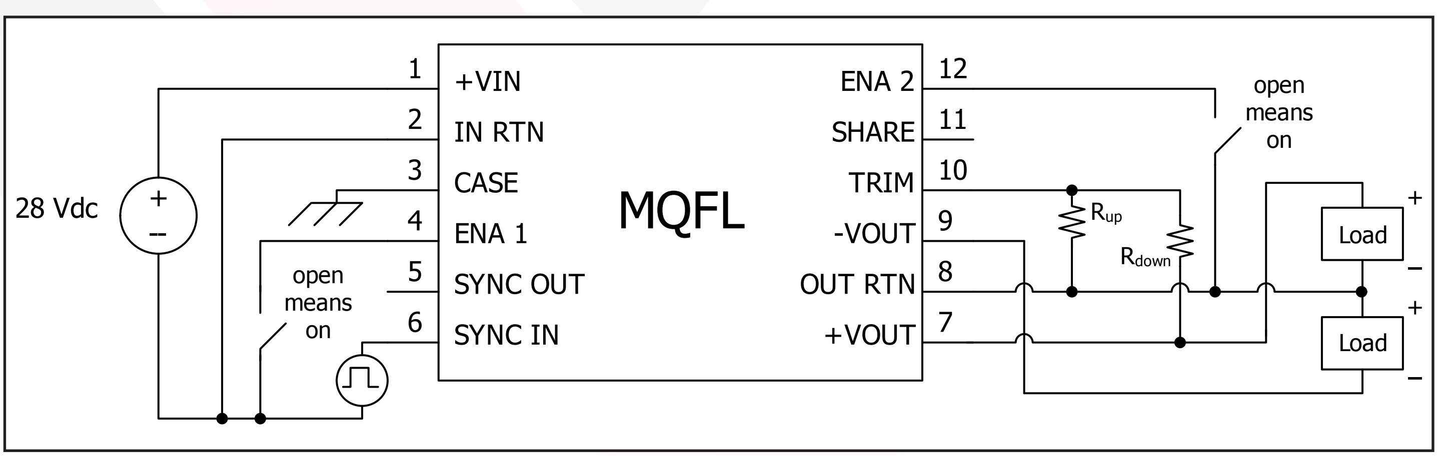


Figure D: Typical connection for output voltage trimming.

prevent the converter from restarting for approximately 300 ms. After the 300 ms delay elapses, if the enable inputs are high and the input voltage is within the operating range, the converter will restart. If the VIN input is brought down to nearly 0 V and back into the operating range, there is no startup inhibit, and the output voltage will rise according to the "Turn-On Delay, Rising Vin" specification.

BACK-DRIVE CURRENT LIMIT: Converters that use MOSFETs as synchronous rectifiers are capable of drawing a negative current from the load if the load is a source of short- or long-term energy. This negative current is referred to as a "back-drive current".

Conditions where back-drive current might occur include paralleled converters that do not employ current sharing, or where the current share feature does not adequately ensure sharing during the startup or shutdown transitions. It can also occur when converters having different output voltages are connected together through either explicit or parasitic diodes that, while normally off, become conductive during startup or shutdown. Finally, some loads, such as motors, can return energy to their power rail. Even a load capacitor is a source of back-drive energy for some period of time during a shutdown transient.

To avoid any problems that might arise due to back-drive current, the MQFL converters limit the negative current that the converter can draw from its output terminals. The threshold for this back-drive current limit is placed sufficiently below zero so that the converter may operate properly down to zero load, but its absolute value (see the Electrical Characteristics page) is small compared to the converter's rated output current.

THERMAL CONSIDERATIONS: Figure 11 shows the suggested Power Derating Curves for this converter as a function of the case temperature and the maximum desired power MOSFET junction temperature. All other components within the converter are cooler than its hottest MOSFET, which at full power is no more than 20 ºC higher than the case temperature directly below this MOSFET.

The Mil-HDBK-1547A component derating guideline calls for a maximum component temperature of 105 ºC. Figure 11 therefore has one power derating curve that ensures this limit is maintained. It has been SynQor's extensive experience that reliable long-term converter operation can be achieved with a maximum component temperature of 125 ºC. In extreme cases, a maximum temperature of 145 ºC is permissible, but not recommended for long-term operation where high reliability is required. Derating curves for these higher temperature limits are also included in Figure 11. The maximum case temperature at which the converter should be operated is 135 ºC.

When the converter is mounted on a metal plate, the plate will help to make the converter's case bottom a uniform temperature. How well it does so depends on the thickness of the plate and on the thermal conductance of the interface layer (e.g. thermal grease, thermal pad, etc.) between the case and the plate. Unless this is done very well, it is important not to mistake the plate's temperature for the maximum case temperature. It is easy for them to be as much as 5-10 ºC different at full power and at high temperatures. It is suggested that a thermocouple be attached directly to the converter's case through a small hole in the plate when investigating how hot the converter is getting. Care must also be made to ensure that there is not a large thermal resistance between the thermocouple and the case due to whatever adhesive might be used to hold the thermocouple in place.

INPUT SYSTEM INSTABILITY: This condition can occur because any DC-DC converter appears incrementally as a negative resistance load. A detailed application note titled "Input System Instability" is available on the SynQor website which provides an understanding of why this instability arises, and shows the preferred solution for correcting it.

CONSTRUCTION AND ENVIRONMENTAL STRESS SCREENING OPTIONS

Screening	Consistent with MIL-STD-883F	C-Grade (specified from 0 °C to +70 °C)	ES-Grade (specified from -45 °C to +100 °C)	HB-Grade (specified from -55 °C to +125 °C)
Element Evaluation		No	Yes	Yes
Internal Visual	IPC-A-610 Class 3	Yes	Yes	Yes
Temperature Cycle	Method 1010	No	Condition B (-55 °C to +125 °C)	Condition C (-65 °C to +150 °C)
Constant Acceleration	Method 2001 (Y1 Direction)	No	500 g	Condition A (5000 g)
Burn-in	Method 1015	24 Hrs @ +125 °C	96 Hrs @ +125 °C	160 Hrs @ +125 °C
Final Electrical Test	Method 5005 (Group A)	+25 °C	-45, +25, +100 °C	-55, +25, +125 °C
Mechanical Seal, Thermal, and Coating Process			Full QorSeal	Full QorSeal
External Visual	Method 2009	Yes	Yes	Yes
Construction Process			QorSeal	QorSeal

MilQor® Hi-Rel converters and filters are offered in three variations of environmental stress screening options. All ES-Grade and HB-Grade MilQor Hi-Rel converters use SynQor's proprietary QorSeal® Hi-Rel assembly process that includes a Parylene-C coating of the circuit, a high performance thermal compound filler, and a nickel barrier gold plated aluminum case. Each successively higher grade has more stringent mechanical and electrical testing, as well as a longer burn-in cycle. The ES- and HB-Grades are also constructed of components that have been procured through an element evaluation process that pre-qualifies each new batch of devices.

MIL-STD-810F Qualification Testing

MIL-STD-810F Test	Method	Description
Fungus	508.5	Table 508.5-I
Altitude	500.4 - Procedure I	Storage: 70,000 ft / 2 hr duration
	500.4 - Procedure II	Operating: 70,000 ft / 2 hr duration; Ambient Temperature
Rapid Decompression	500.4 - Procedure III	Storage: 8,000 ft to 40,000 ft
Acceleration	513.5 - Procedure II	Operating: 15 g
Salt Fog	509.4	Storage
High Temperature	501.4 - Procedure I	Storage: 135 °C / 3 hrs
	501.4 - Procedure II	Operating: 100 °C / 3 hrs
Low Temperature	502.4 - Procedure I	Storage: -65 °C / 4 hrs
	502.4 - Procedure II	Operating: -55 °C / 3 hrs
Temperature Shock	503.4 - Procedure I - C	Storage: -65 °C to 135 °C; 12 cycles
Rain	506.4 - Procedure I	Wind Blown Rain
Immersion	512.4 - Procedure I	Non-Operating
Humidity	507.4 - Procedure II	Aggravated cycle @ 95% RH (Figure 507.5-7 aggravated temp - humidity cycle, 15 cycles)
Random Vibration	514.5 - Procedure I	10 - 2000 Hz, PSD level of 1.5 g^2/Hz (54.6 g_{rms}), duration = 1 hr/axis
Shock	516.5 - Procedure I	20 g peak, 11 ms, Functional Shock (Operating no load) (saw tooth)
	516.5 - Procedure VI	Bench Handling Shock
Sinusoidal vibration	514.5 - Category 14	Rotary wing aircraft - helicopter, 4 hrs/axis, 20 g (sine sweep from 10 - 500 Hz)
Sand and Dust	510.4 - Procedure I	Blowing Dust
	510.4 - Procedure II	Blowing Sand

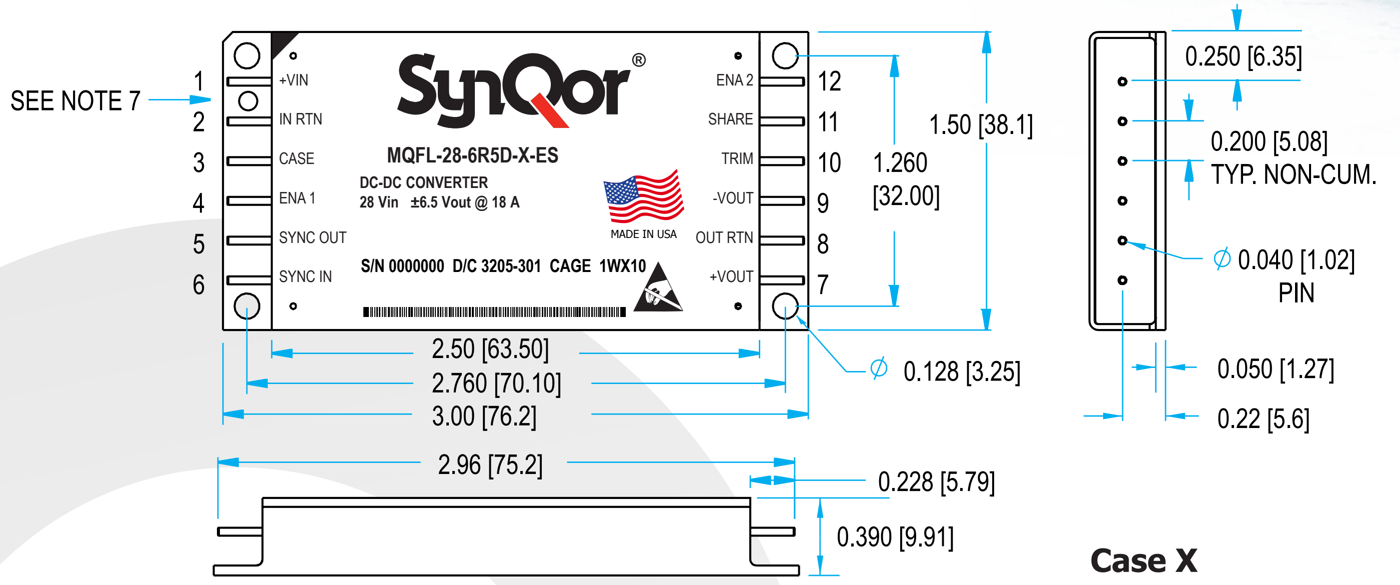
First Article Testing consistent with MIL-STD-883F

MIL-STD-883F Test	Method	Description
Electrical Tests	5005	
Physical Dimensions test	2016	
Resistance to Solvents test	2015.13	
Solderability test	2003.8	
Lead Integrity test	2004.5	
Salt Atmosphere test	1009.8	Condition "A"
Adhesion of Lead Finish test	2025.4	
Altitude Operation test	1001	Condition "C"
ESD Sensitivity	3015.7	Class 2
Stabilization Bake test	1008.2	Condition "C"
Vibration Fatigue test	2005.2	Condition "A"
Random Vibration test	2026	Condition "II K"
Sequential Test Group #1		
Life Test – Steady State test	1005.8	
Life Test – Intermittent Duty test	1006	
Sequential Test Group #2		
Temperature Cycle test	1010.8	Condition "C"
Constant Acceleration test	2001.2	Condition "A"
Sequential Test Group #3		
Thermal Shock test	1011.9	Condition "B"
Temperature Cycle test	1010.8	Condition "C"
Moisture Resistance test	1004.7	With Sub cycle
Sequential Test Group #4		
Mechanical Shock test	2002.4	Condition "B"
Variable Frequency Vibration test	2007.3	Condition "A"

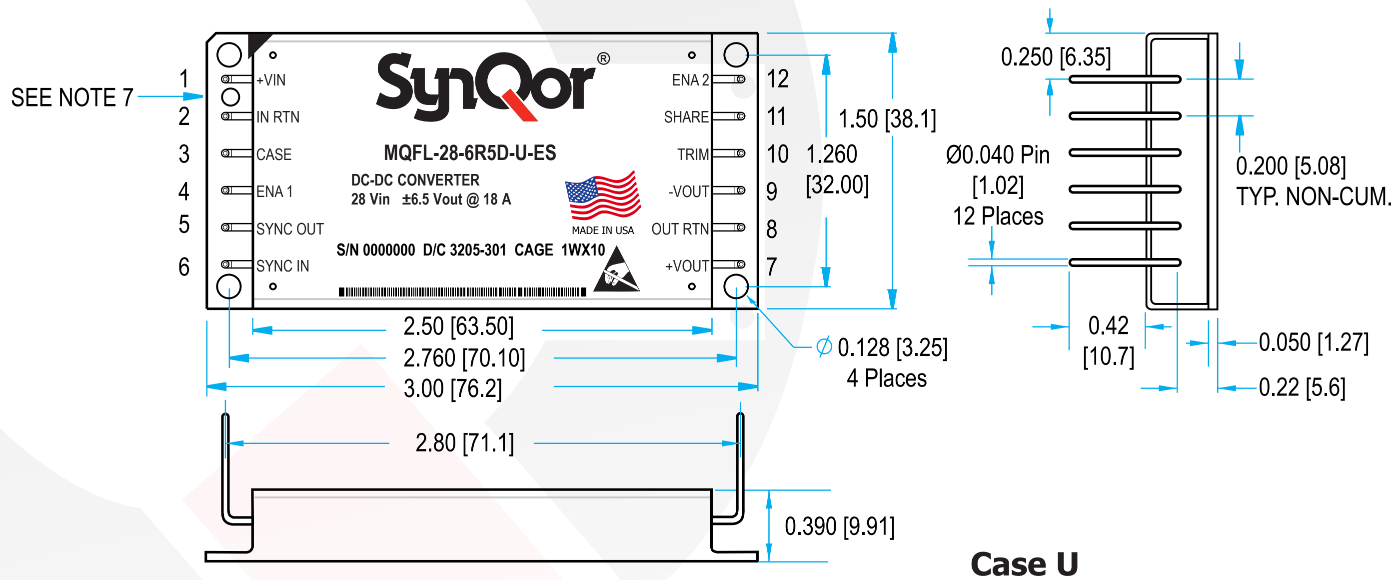
SynQor®

Mechanical Diagrams

MQFL-28-6R5D
Output: ±6.5 V
Current: 18 A Total



Case X



Case U

NOTES

1) Pins 0.040" (1.02 mm) diameter
2) Pin Material: Copper Alloy
   Finish: Gold over Nickel plating, followed by Sn/Pb solder dip
3) All dimensions in inches (mm) Tolerances: x.xx +/-0.02 in. (x.x +/-0.5 mm)
   x.xxx +/-0.010 in. (x.xx +/-0.25 mm)
4) Weight: 2.8 oz (78.5 g) typical
5) Workmanship: Meets or exceeds IPC-A-610 Class III
6) Print Labeling on Top Surface per Product Label Format Drawing
7) Pin 1 identification hole, not intended for mounting (case X and U)
8) Baseplate flatness tolerance is 0.004" (.10 mm) TIR for surface.

PIN DESIGNATIONS

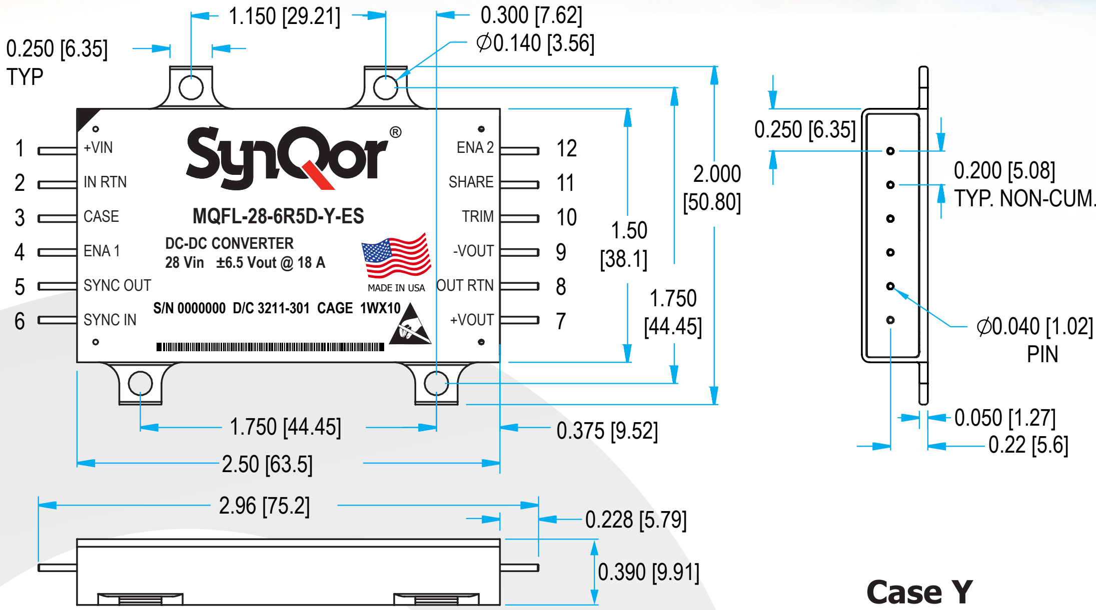
Pin #	Function
1	Positive input
2	Input return
3	Case
4	Enable 1
5	Sync output
6	Sync input

Pin #	Function
7	Positive output
8	Output return
9	Negative Output
10	Trim
11	Share
12	Enable 2

SynQor®

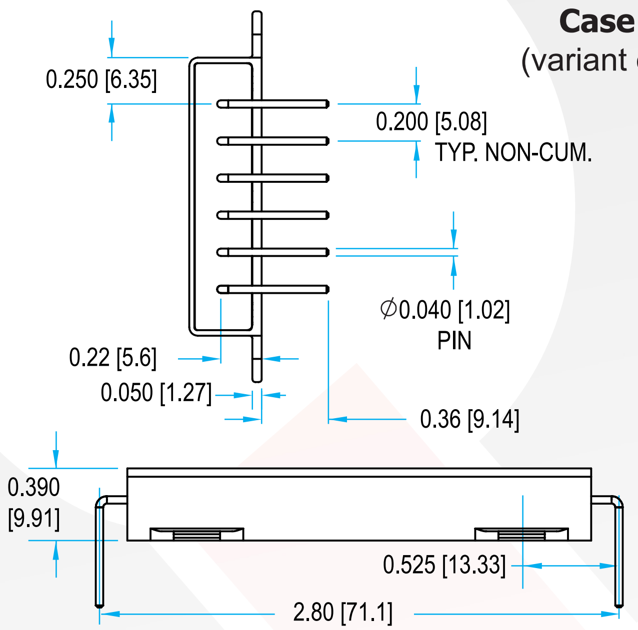
Mechanical Diagrams

MQFL-28-6R5D
Output: ±6.5 V
Current: 18 A Total

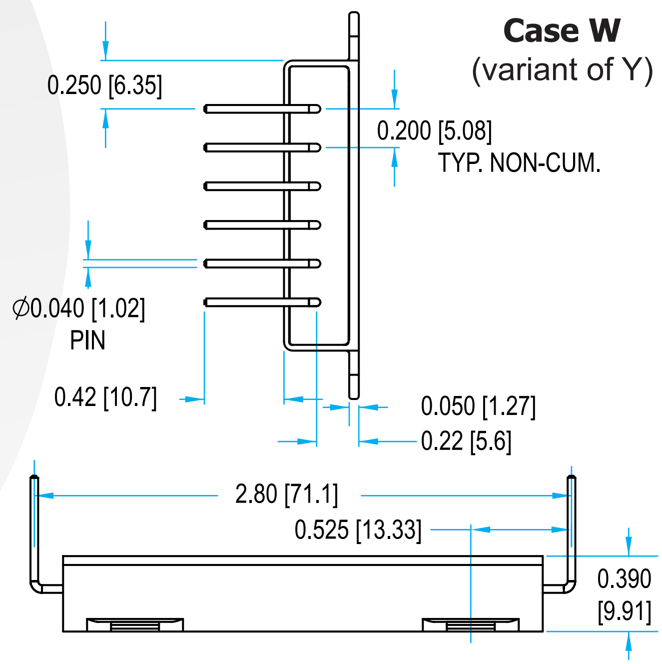


Case Y

Case Z
(variant of Y)



Case W
(variant of Y)



NOTES

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2) Pin Material: Copper Alloy
   Finish: Gold over Nickel plating, followed by Sn/Pb solder dip
3) All dimensions in inches (mm) Tolerances: x.xx +/-0.02 in. (x.x +/-0.5 mm)
   x.xxx +/-0.010 in. (x.xx +/-0.25 mm)
4) Weight: 2.8 oz (78.5 g) typical
5) Workmanship: Meets or exceeds IPC-A-610 Class III
6) Print Labeling on Top Surface per Product Label Format Drawing
7) Pin 1 identification hole, not intended for mounting (case X and U)
8) Baseplate flatness tolerance is 0.004" (.10 mm) TIR for surface.

PIN DESIGNATIONS

Pin #	Function
1	Positive input
2	Input return
3	Case
4	Enable 1
5	Sync output
6	Sync input

Pin #	Function
7	Positive output
8	Output return
9	Negative Output
10	Trim
11	Share
12	Enable 2

MQFL-28-6R5D
Output: ±6.5 V
Current: 18 A Total

Ordering Information

MilQor Converter FAMILY MATRIX

The tables below show the array of MilQor converters available. When ordering SynQor converters, please ensure that you use the complete part number according to the table in the last page. Contact the factory for other requirements.

	Single Output											Dual Output †		
Full Size	1.5 V (1R5S)	1.8 V (1R8S)	2.5 V (2R5S)	3.3 V (3R3S)	5 V (05S)	6 V (06S)	7.5 V (7R5S)	9 V (09S)	12 V (12S)	15 V (15S)	28 V (28S)	5 V (05D)	12 V (12D)	15 V (15D)
MQFL-28 16-40 Vin Cont. 16-50 Vin 1 s Trans.* Absolute Max Vin = 60 V	40 A	40 A	40 A	30 A	24 A	20 A	16 A	13 A	10 A	8 A	4 A	24 A Total	10 A Total	8 A Total
MQFL-28E 16-70 Vin Cont. 16-80 Vin 1 s Trans.* Absolute Max Vin =100 V	40 A	40 A	40 A	30 A	24 A	20 A	16 A	13 A	10 A	8 A	4 A	24 A Total	10 A Total	8 A Total
MQFL-28 V 16-40 Vin Cont. 5.5-50 Vin 1 s Trans.* Absolute Max Vin = 60 V	40 A	40 A	40 A	30 A	20 A	17 A	13 A	11 A	8 A	6.5 A	3.3 A			
MQFL-28 VE 16-70 Vin Cont. 5.5-80 Vin 1 s Trans.* Absolute Max Vin = 100 V	40 A	40 A	40 A	30 A	20 A	17 A	13 A	11 A	8A	6.5A	3.3A			
MQFL-270 155-400 Vin Cont. 155-475 Vin 1 s Trans.* Absolute Max Vin = 550 V	40A	40A	40A	30A	24A	20A	16A	13 A	10A	8 A	4 A	24 A Total	10 A Total	8 A Total
MQFL-270L 65-350 Vin Cont. 65-475 Vin 1 s Trans.* Absolute Max Vin = 550 V	40 A	40 A	30 A	22 A	15 A	12 A	10 A	8 A	6 A	5 A	2.7 A	15 A Total	6 A Total	5 A Total

	Single Output											Dual Output †		
Half Size	1.5 V (1R5S)	1.8 V (1R8S)	2.5 V (2R5S)	3.3 V (3R3S)	5 V (05S)	6 V (06S)	7.5 V (7R5S)	9 V (09S)	12 V (12S)	15 V (15S)	28 V (28S)	5 V (05D)	12 V (12D)	15 V (15D)
MQHL-28 16-40 Vin Cont. 16-50 Vin 1 s Trans.* Absolute Max Vin = 60 V	20 A	20 A	20 A	15 A	10 A	8 A	6.6 A	5.5 A	4 A	3.3 A	1.8 A	10 A Total	4 A Total	3.3 A Total
MQHL-28E 16-70 Vin Cont. 16-80 Vin 1 s Trans.* Absolute Max Vin =100 V	20 A	20 A	20 A	15 A	10 A	8 A	6.6 A	5.5 A	4 A	3.3 A	1.8 A	10 A Total	4 A Total	3.3 A Total
MQHR-28 16-40 Vin Cont. 16-50 Vin 1 s Trans.* Absolute Max Vin = 60 V	10 A	10 A	10 A	7.5 A	5 A	4 A	3.3 A	2.75 A	2 A	1.65 A	0.9 A	5 A Total	2 A Total	1.65 A Total
MQHR-28E 16-70 Vin Cont. 16-80 Vin 1 s Trans.* Absolute Max Vin = 100 V	10 A	10 A	10 A	7.5 A	5 A	4 A	3.3 A	2.75 A	2 A	1.65 A	0.9 A	5 A Total	2 A Total	1.65 A Total

Check with factory for availability.

†80% of total output current available on any one output.
*Converters may be operated at the highest transient input voltage, but some component electrical and thermal stresses would be beyond MIL-HDBK-1547A guidelines.

MQFL-28-6R5D
Output: ±6.5 V
Current: 18 A Total

PART NUMBERING SYSTEM

The part numbering system for SynQor's MilQor DC-DC converters follows the format shown in the table below.

Not all combinations make valid part numbers, please contact SynQor for availability. See the Product Summary web page for more options.

Example: MQFL-28-6R5D-Y-ES

Model Name	Input Voltage Range	Output Voltage(s)		Package Outline/ Pin Configuration	Screening Grade
		Single Output	Dual Output		
MQFL MQHL MQHR	28 28E 28V 28VE 270 270L	1R5S 1R8S 2R5S 3R3S 05S 06S 6R5S 7R5S 08S 09S 12S 15S 28S	05D 6R5D 12D 15D	U X Y W Z	C ES HB

APPLICATION NOTES

A variety of application notes and technical white papers can be downloaded in pdf format from the SynQor website.

Contact SynQor for further information and to order:

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Fax: 978-849-0602
E-mail: mqnbofae@synqor.com
Web: www.synqor.com
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Boxborough, MA 01719
USA

PATENTS

SynQor holds numerous U.S. patents, one or more of which apply to most of its power conversion products. Any that apply to the product(s) listed in this document are identified by markings on the product(s) or on internal components of the product(s) in accordance with U.S. patent laws. SynQor's patents include the following:

6,896,526 6,927,987 7,050,309 7,085,146

7,765,687 7,787,261 8,149,597 8,644,027

Warranty

SynQor offers a two (2) year limited warranty. Complete warranty information is listed on our website or is available upon request from SynQor.